

BGM1033N7

GPS and GLONASS Front-End Module

Data Sheet

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BGM1033N7 GPS and GLONASS Front-End Module

Revision History: 2011-07-18, Revision 3.2

Previous Revision: 2011-06-30, Revision 3.1

Page	Subjects (major changes since last revision)
9	Updated value for Out-of-band 3rd Order Intercept Point
16	Updated carrier tape drawing

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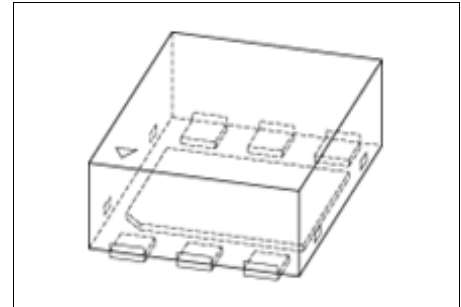
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1 Features

Main features:

- Operating frequencies: 1575.42 MHz and 1598.06-1605.38 MHz
- High Gain: 14.8 dB
- Low Noise Figure (GPS): 1.65 dB
- Low current consumption: 4.0 mA
- Out-of-band rejection in cellular bands: > 43 dBc
- Input compression point in cellular bands: 30 dBm
- Supply voltage: 1.5 V to 3.6 V
- Tiny TSNP-7-10 leadless package (2.3 x 1.7 x 0.73 mm³)
- RF output internally matched to 50 Ω
- IEC ESD contact discharge of RF input pin: 6 kV
- Only 3 external SMD parts
- RoHS compliant package (Pb-free)



Description

The BGM1033N7 is a combination of a low-insertion-loss pre-filter with Infineon's high performance low noise amplifier (LNA) for Global Positioning System (GPS) and Globalnaya Navigatsionnaya Sputnikovaya Sistema (GLONASS) applications. Both, GPS and GLONASS frequency bands, can be used at the same time. Through the low insertion loss of the filter, the BGM1033N7 provides 14.8 dB gain, 1.65 dB noise figure and high linearity performance. In addition BGM1033N7 provides very high out-of-band attenuation in conjunction with a high input compression point. It can withstand IEC ESD contact discharge at the RF input as high as 6 kV. Its current consumption is as low as 4.0 mA. It operates over the 1.5 V to 3.6 V supply voltage range.

Product Name	Package	Marking
BGM1033N7	TSNP-7-10	M33

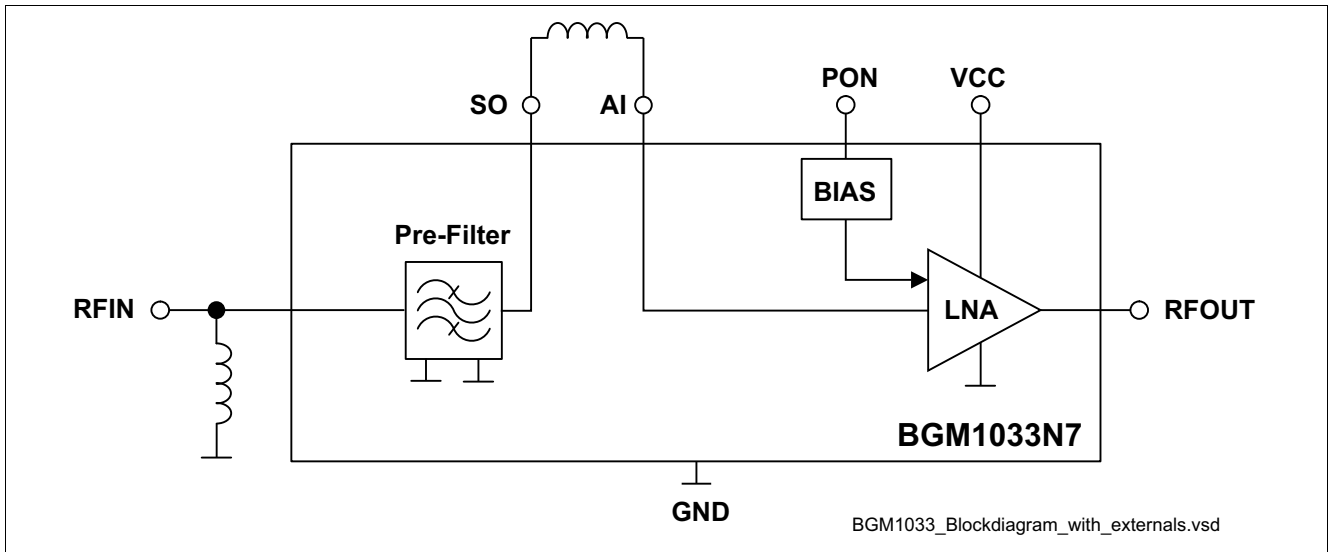


Figure 1 Block Diagram with Main External Components

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at pin PON to GND	V_{PON}	-0.3	–	3.6	V	–
Voltage at pin VCC to GND	V_{CC}	-0.3	–	3.6	V	–
Voltage at pin RFIN to GND	V_{RFIN}	-3	–	3	V	–
Voltage at pin SO to GND	V_{BO}	-3	–	3	V	–
Voltage at pin AI to GND	V_{AI}	-0.3	–	0.75	V	–
Voltage at pin RFOUT to GND	V_{RFOUT}	-0.3	–	$V_{CC}+0.3$	V	–
Current into pin VCC	I_{VCC}	–	–	25	mA	–
RF input power inband	P_{IN}	–	–	0	dBm	Continuous wave signal $f = 1575.42$ MHz 50 Ω source and load impedances
RF input power out of band	$P_{IN,OB}$	–	–	25	dBm	Continuous wave signal $f = 50 - 1460$ MHz and 1710 - 4000 MHz 50 Ω source and load impedances
Total power dissipation	P_{tot}	–	–	90	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{stg}	-65	–	150	°C	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 ESD Integrity

Table 2 ESD Integrity

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD capability HBM of pins 1, 2, 5 and 6	V_{ESD1}	–	–	2	kV	According to JESD22-A114
ESD capability HBM of pins 3 and 4	V_{ESD2}	–	–	300	V	According to JESD22-A114
ESD contact discharge capability of RF input pin 3	V_{ESD3}	–	–	6	kV	According to IEC61000-4-2
ESD capability MM of RF input pin 3 and pre-filter output pin 4	V_{ESD4}	–	–	50	V	According to JESD22-A115

2.3 RF Characteristics

Table 3 Typical Characteristics: $T_A = 25\text{ }^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$, $V_{PON,ON} = 2.7\text{ V}$, $V_{PON,OFF} = 0\text{ V}^1)$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	1.5	2.7	3.6	V	–
Supply Current	I_{CC}	–	4.0	–	mA	ON-Mode
		–	0.2	3	μA	OFF-Mode
Power On Control Voltage	V_{PON}	1.0	–	V_{CC}	V	ON-Mode
		0	–	0.4	V	OFF-Mode
Power On Control Current	I_{PON}	–	9.5	–	μA	ON-Mode
		–	–	1	μA	OFF-Mode
Power Gain Settling Time ²⁾	t_S	–	5	–	μs	OFF- to ON-Mode
		–	5	–	μs	ON- to OFF-mode
Passband Parameters @ $f = 1575.42, 1598.06$ - 1605.38 MHz	–	–	–	–	–	–
Insertion Power Gain	$ S_{21} ^2$	–	14.8	–	dB	
Noise Figure GPS ³⁾	NF	–	1.65	2.2	dB	$Z_S = 50\ \Omega$ $f = 1575.42\text{ MHz}$
Noise Figure GLONASS ³⁾	NF	–	2.0	2.5	dB	$Z_S = 50\ \Omega$ $f = 1598.06$ - 1605.38 MHz
Group Delay Ripple	T_G	–	8	–	ns	$f = 1575\text{ MHz}$, $1598 - 1605\text{ MHz}$
Input Return Loss	RL_{IN}	–	15	–	dB	–
Output Return Loss	RL_{OUT}	–	15	–	dB	–
Reverse Isolation	$1/ S_{12} ^2$	–	22	–	dB	–
Inband Input 3rd Order Intercept Point	IIP_3	–	-6	–	dBm	$f_1 = 1575.42\text{ MHz}$ $f_2 = f_1 + 1\text{ MHz}$
Inband Input 1 dB Compression Point	IP_{1dB}	–	-6	–	dBm	$f_1 = 1575.42\text{ MHz}$
Out-of-band 3rd Order Intercept Point ⁴⁾	IIP_{3OOB}	–	60	–	dBm	$f_1 = 1712.7\text{ MHz}$ $f_2 = 1850\text{ MHz}$
Out-of-band Input 1 dB Compression Point ⁵⁾	IP_{1dB_900M}	–	30	–	dBm	$f_1 = 900\text{ MHz}$
Out-of-band Input 1 dB Compression Point ⁵⁾	IP_{1dB_1710M}	–	30	–	dBm	$f_1 = 1710\text{ MHz}$
Stopband Parameters	–	–	–	–	–	–
Rejection ⁶⁾	Rej_{750M}	–	54	–	dBc	$f = 750\text{ MHz}$
Rejection ⁶⁾	Rej_{900M}	–	53	–	dBc	$f = 806\text{ MHz} - 928\text{ MHz}$
Rejection ⁶⁾	Rej_{1800M}	–	43	–	dBc	$f = 1710\text{ MHz} - 1980\text{ MHz}$

Table 3 Typical Characteristics: $T_A = 25\text{ °C}$, $V_{CC} = 2.7\text{ V}$, $V_{PON,ON} = 2.7\text{ V}$, $V_{PON,OFF} = 0\text{ V}$ ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rejection ⁶⁾	Rej_{2400M}	–	54	–	dBc	$f = 2400\text{ MHz} - 2500\text{ MHz}$
Stability	k	–	>1	–	–	$f = 20\text{ MHz} - 20\text{ GHz}$

- 1) Measured on application board including PCB losses (unless noted otherwise)
- 2) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode
- 3) PCB and connector losses subtracted, verified on AQL base
- 4) Input power = +10 dBm for each tone
- 5) Guaranteed by device design, not measured in production
- 6) Rejection = $|1/|S_{21}|^2 \text{ at stopband frequency}| + |1/|S_{21}|^2 \text{ at } 1575.42\text{ MHz}|$

3 Application Circuit and Block Diagram

3.1 Application Circuit Schematic

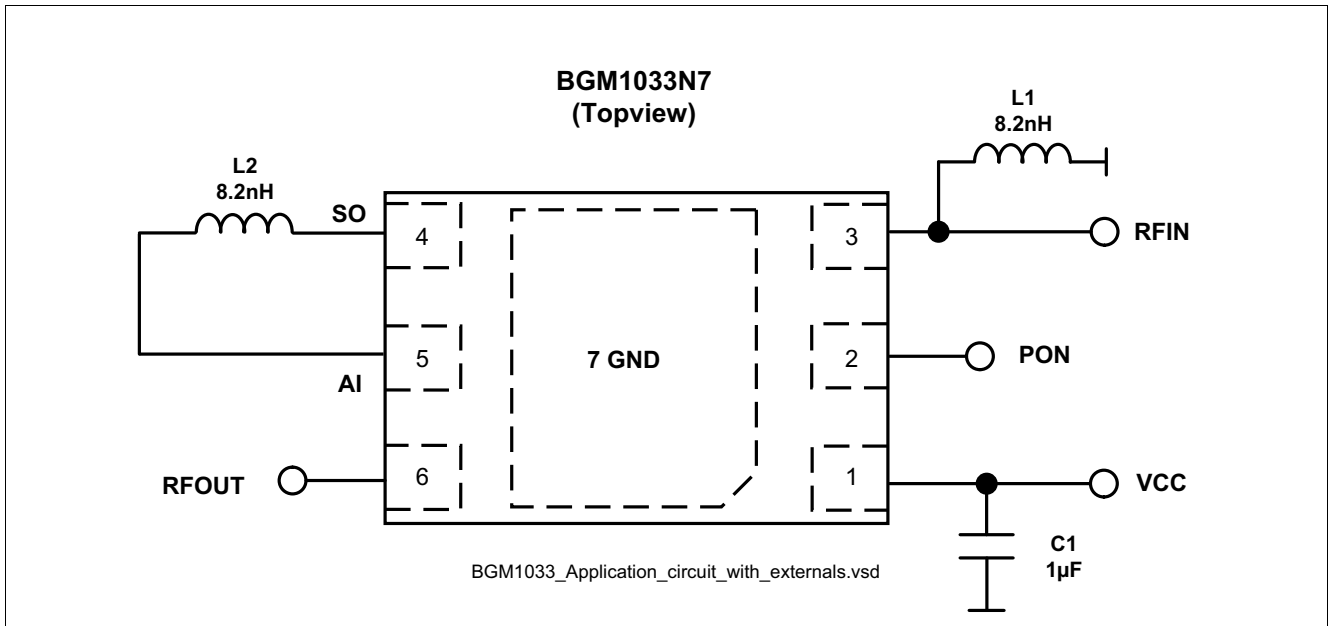


Figure 2 Application Circuit with Chip Outline (top view)

Table 4 Parts List

Part Number	Part Type	Manufacturer	Size	Comment
C1	Chip capacitor	Various	0402	Supply filtering
L1	Chip inductor	muRata LQW15A	0402	Matching + ESD protection inductor
L2	Chip inductor	muRata LQW15A	0402	Input Matching
N1	BGM1033N7	Infineon	TSNP-7-10	GPS FE-Module

3.2 Pin Description

Table 5 Pin Definition and Function

Pin No.	Name	Pin Type	Buffer Type	Function
1	VCC			Power Supply
2	PON			Power On/Off
3	RFIN			RF Input
4	SO			Pre-Filter Output
5	AI			LNA Input
6	RFOUT			RF Output
7	GND			DC and RF ground

3.3 Application Board

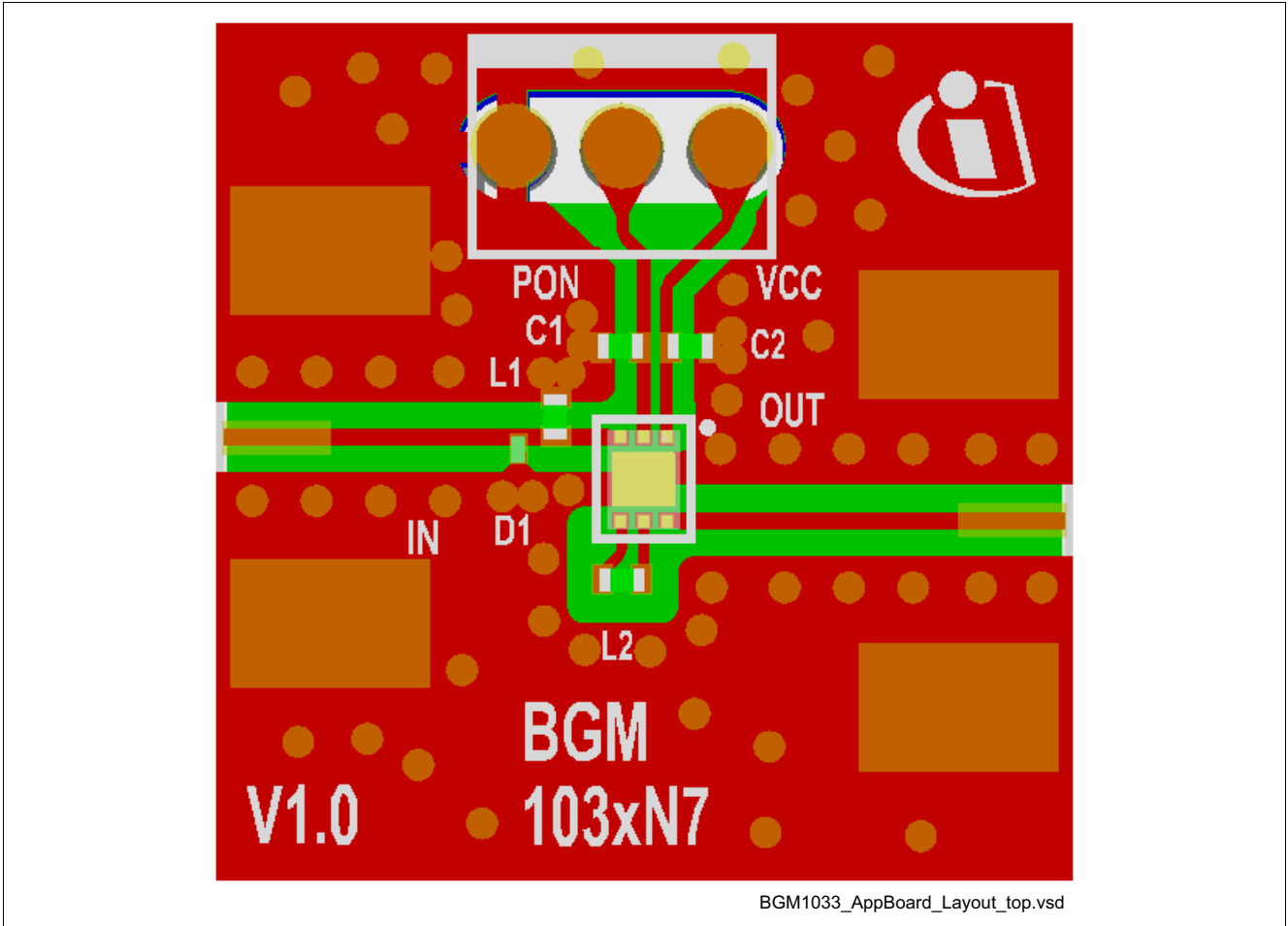


Figure 3 Top view of Application Board

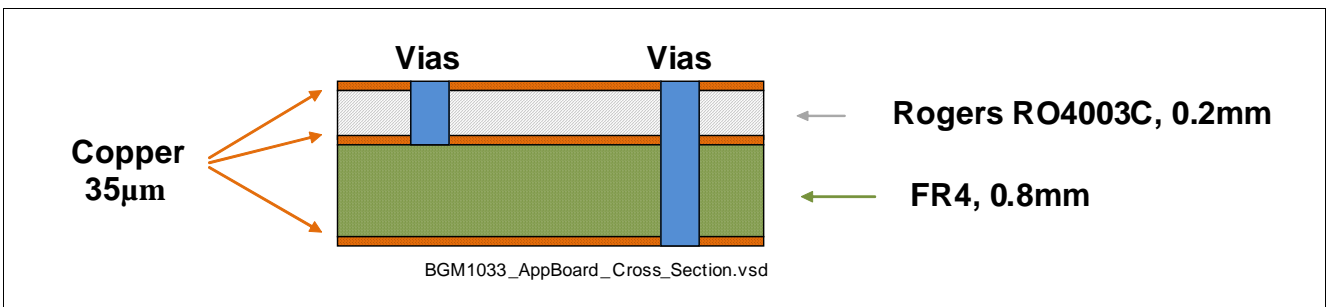


Figure 4 Cross-Section view of Application Board

4 Package Information

4.1 Package Footprint

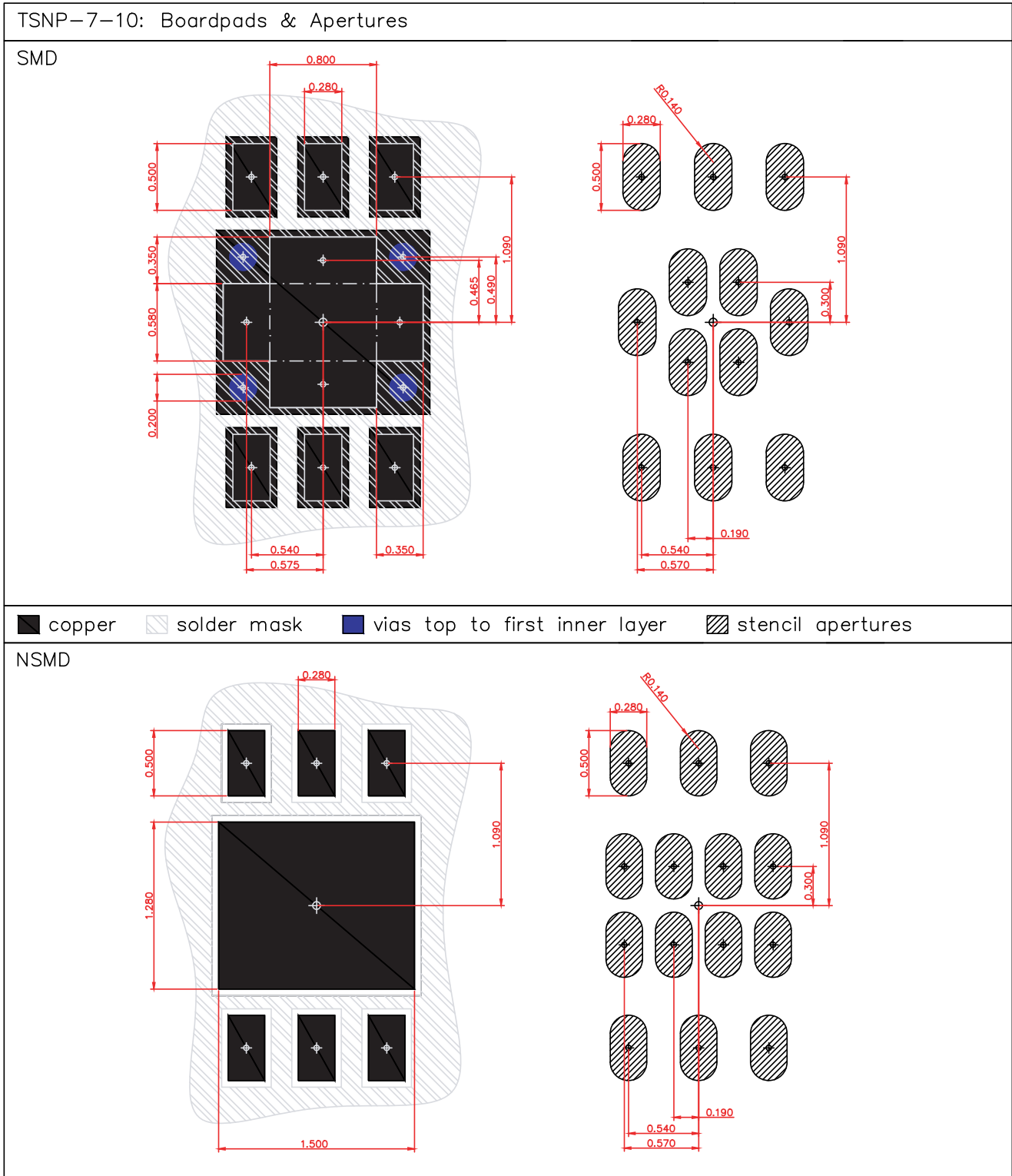


Figure 5 Recommended PCB Footprint for the TSNP-7-10 Package (subject to be changed)

4.2 Package Dimensions

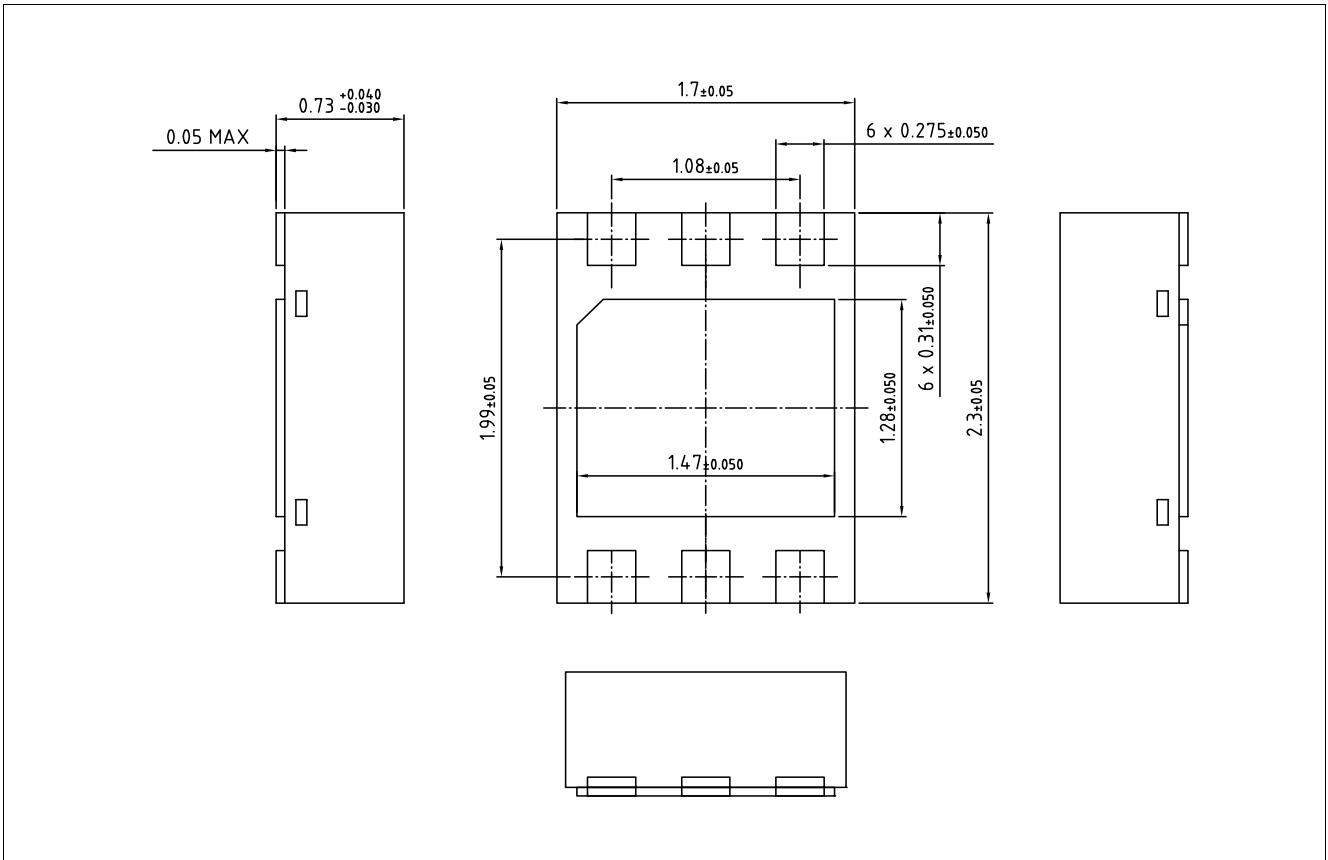


Figure 6 TSNP-7-10 Package Outline (bottom and side views)

4.3 Product Marking Pattern

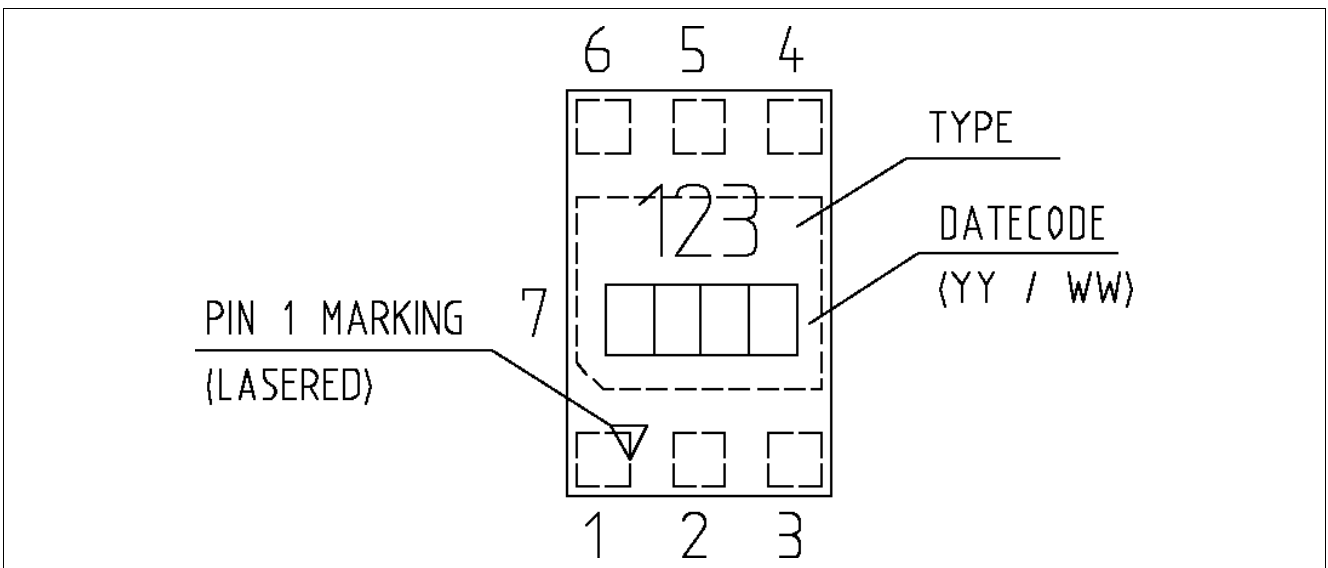


Figure 7 Marking Pattern (top view)

5 Packing Information

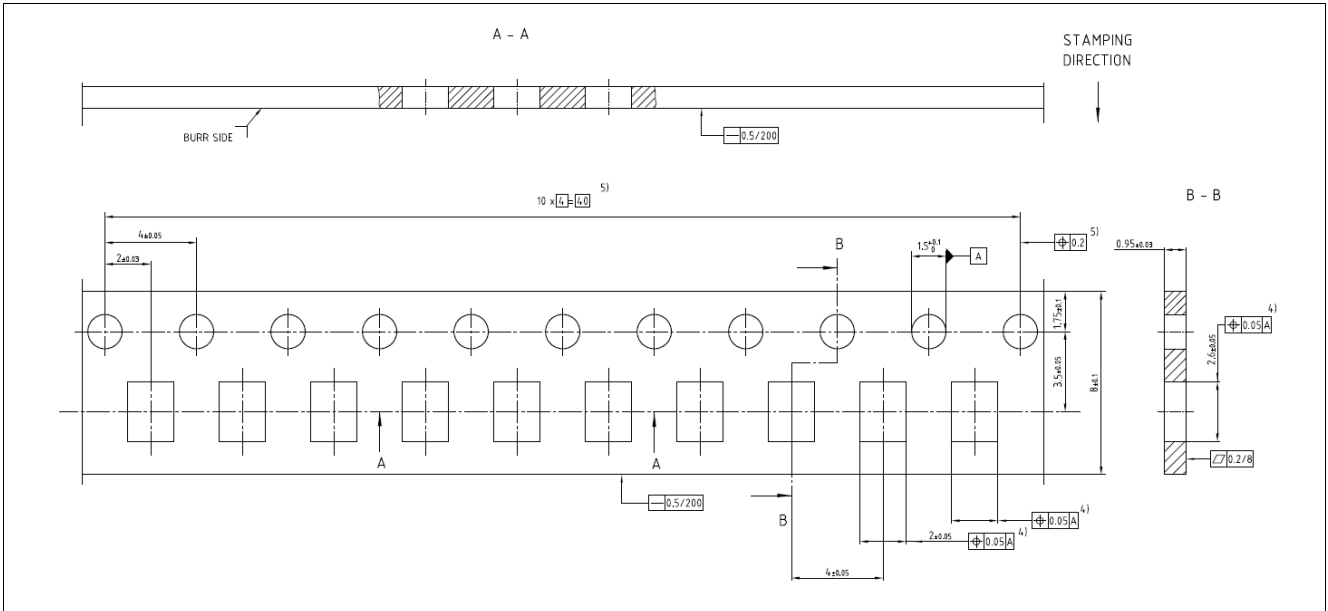


Figure 8 TSNP-7-10 Carrier tape

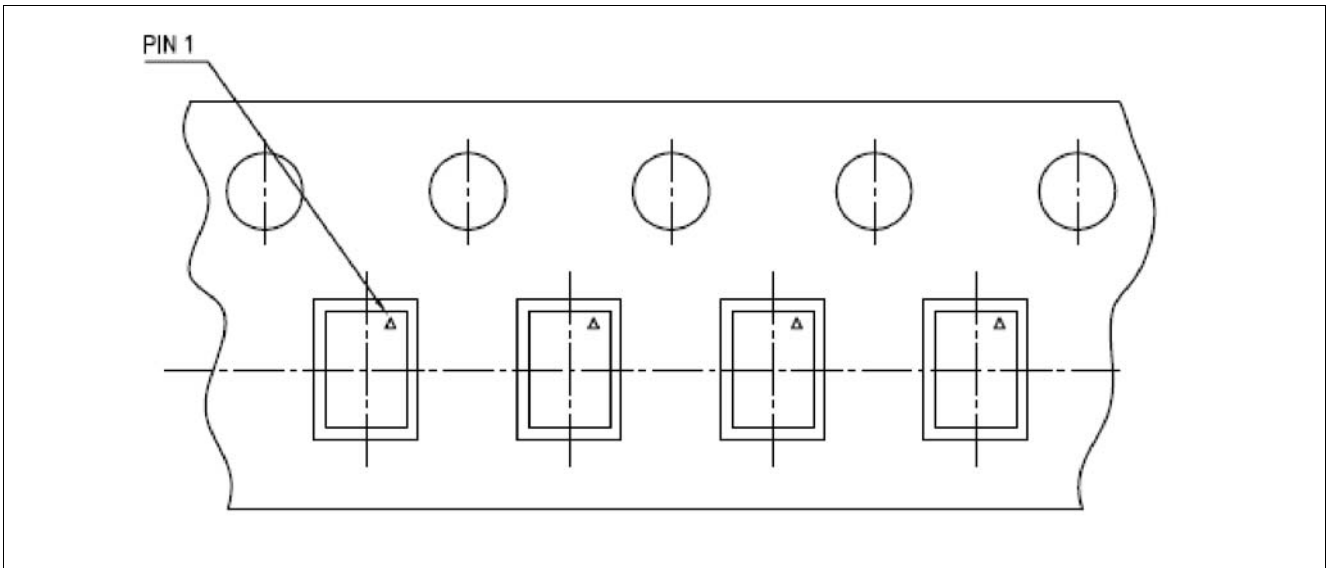


Figure 9 TSNP-7-10 Pin 1 orientation in tape

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